IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application. An identifier indicating the status of each claim is provided.

Listing of Claims:

1. (Currently Amended) A signal processor for processing a predetermined unit of input data containing a variable length code, header information and information providing the active length of the variable length code, said signal processor comprising:

input means for inputting the input data;

start detecting means for detecting a start of the predetermined unit of the input data, in which the predetermined unit corresponds to a frame;

means for receiving a frame end signal that has been generated based on said header information and is synchronized with end of frame data, said frame end signal being indicative of the end of each frame;

end detecting means for detecting the end of a respective frame based on the frame end signal; and

signal processing means for executing an action on the variable length code active at the start detected by said start detecting means, for making the action on the variable length code inactive at the end detected by said end detecting means, and for initializing the state of the action on the variable length code at the end detected by said end detecting means,

wherein the level of an enable signal is ~~altered between~~ set as a high level indicating valid data once a start code is detected and is set as a low level indicating invalid data

once a frame end signal is detected ~~based on a frame end signal and a result of a detected start code~~,

wherein, when the start of a frame is not detected, the data received after the frame end signal of the previous frame and before the start of a next frame is not processed and is designated invalid allowing immediate processing of the next frame thereby eliminating invalid data and reducing further lost data.

2. (Original) A signal processor according to Claim 1, wherein the input data comprises MPEG encoded data.

3. (Original) A signal processor according to Claim 1, further comprising recording means for recording the output of said signal processing means.

4. (Currently Amended) A signal processing method for processing a predetermined unit of input data containing a variable length code, header information and information providing the active length of the variable length code, said signal processing method comprising the steps of:

inputting the input data;

detecting a start of the predetermined unit of the input data input in said inputting step, in which the predetermined unit corresponds to a frame;

receiving a frame end signal that has been generated based on said header information and is synchronized with end of frame data, said frame end signal being indicative of the end of each frame;

detecting the end of a respective frame based on the frame end signal; and

performing processes to execute an action on the variable length code active at the start detected in said start detecting step, to make the action on the variable length code inactive at the end detected in said end detecting step, and to initialize the state of the action on the variable length code at the end detected in said end detecting step,

wherein the level of an enable signal is ~~altered between~~ set as a high level indicating valid data once a start code is detected and is set as a low level indicating invalid data once a frame end signal is detected ~~based on a frame end signal and a result of a detected start code~~,

wherein, when the start of a frame is not detected, the data received after the frame end signal of the previous frame and before the start of a next frame is not processed and is designated invalid allowing immediate processing of the next Frame thereby eliminating invalid data and reducing further lost data.

5. (Original) A signal processing method according to Claim 4, further comprising the step of recording the result of said process performing step.

6. (Previously Presented) The signal processor according to claim 1, wherein the means for receiving includes a flip-flop circuit.

7. (Currently Amended) A method for processing frames of data containing a variable length code, header information and information providing the active length of the variable length code, said method comprising:

generating a frame end signal based on said header information;

synchronizing a frame end signal with end of frame data that indicates an end of each frame;

processing each frame until the end of frame data is detected;

skipping processing data of a period of time, the period of time being from the end of frame data to a subsequent start signal;

detecting a start code for a corrected stream of data;

re-initiating the processing step as a function of the detecting step; and

designating data received after the frame end signal and before the start of a next frame invalid,

wherein the level of an enable signal is ~~altered between~~ set as a high level indicating valid data once a start code is detected and is set as a low level indicating invalid data once a frame end signal is detected ~~based on a frame end signal and a result of a detected start code~~,

wherein, when the start of a frame is not detected, the data received after the frame end signal of the previous frame and before the start of a next frame is not processed and is designated invalid allowing immediate processing of the next frame thereby eliminating invalid data and reducing further lost data.